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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,778	01/09/2001	Jun Koyama	07977/108002/US3190D1	8473

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EXAMINER	
DUONG, TAI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/757,778	KOYAMA ET AL.	
	Examiner	Art Unit	
	Tai Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23 and 31-36* is/are allowed.

6)☒ Claim(s) *1-3,6,7,9,13,14,18,19,21,22,24,28-30 and 40-42* is/are rejected.

7)☒ Claim(s) *4,5,8,10-12,15-17,20,25-27,37-39 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/770,785.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/2/03, 4/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 9/2/03 has been entered.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6, 7, 9, 13, 14, 18, 19, 21, 22 and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 05-158015 (AK) cited by Applicant.

Note Figs. 1, 2, 4-6 and especially Fig. 3 which identically disclose the claimed semiconductor device and method including a pattern 41 comprising a same material as the bus line LG and provided in a same layer as the bus line, wherein the pattern is provided *adjacent to* a side edge of the substrate, and wherein the bus line is apart from the pattern and the side edge of said substrate. The term "adjacent" is broadly interpreted as "close" or "near by". See discussions of the remainder of the recited features in the text. It is noted that US 5,327,267 is the English equivalent of JP 05-158015.

Claims 24 and 40-42 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 05-232511 (AL) cited by Applicant.

Note Figs. 1-3 and paragraphs 0017-0032 of the English translation which disclose all the recited steps of the instant claims, such as cutting the bus line (2, 4) from the short ring 9 without cutting said the TFT substrate to leave behind a pattern over the TFT substrate, the pattern being same as at least a part of the short ring while the pattern is free from a shorting function (Fig. 3); bonding the TFT substrate and a counter substrate together; and cutting the TFT substrate and said counter substrate along a common plane (Fig. 2) , wherein the bus line cut from the short ring is apart from the pattern and the side edge of said TFT substrate (Fig. 3).

Claims 23 and 31-36 are allowed over the prior art of record because none of the prior art discloses or suggests a method comprising the steps of cutting the bus line from the short ring without cutting the substrate to leave behind a pattern over the substrate, the pattern being same as at least a part of the short ring while the pattern is free from a shorting function; and forming a sealant material over the substrate *after the cutting step*, wherein the bus line cut from the short ring is apart from the pattern and the side edge of said substrate.

Claims 4, 5, 8, 10-12, 15-17, 20, 25-27, 37-39 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 4, 5, 8, 10-12, 15-17, 20, 25-27, 37-39 and 43 are allowed over the prior art of record because none of the prior art discloses or suggests the features "a driver thin film transistor provided over said substrate and forming a driver circuit for driving said pixel thin film transistor; and a control circuit for controlling said driver circuit, wherein said control circuit is disposed at a control circuit accommodation portion of said substrate, said control circuit accommodation portion being thinner than other portions of said substrate", "a driver thin film transistor provided over said substrate and forming a driver circuit for driving said pixel thin film transistor; and a control circuit for controlling said driver circuit, wherein said control circuit is provided in said sealant material", "a driver thin film transistor provided over said substrate and forming a driver circuit for driving said pixel thin film transistor; and a control circuit for controlling said driver circuit, wherein said control circuit is provided over said substrate and adjacent to an opposite side edge of said substrate to said pattern", "packing a control circuit over said substrate for controlling a driver circuit made up of a driver thin film transistor, said driver thin film transistor being formed over said substrate for driving said pixel thin film transistor; and sealing said control circuit in said sealant material", "thinning a control circuit accommodation portion of said substrate to install therein a control circuit for controlling a driver circuit made up of a driver thin film transistor, said driver thin film transistor being formed over said substrate for driving said pixel thin film transistor".

Any inquiry concerning this communication should be directed to Tai Duong at telephone number (571) 272-2291.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

TOAN TON
PRIMARY EXAMINER

TVD

05/04